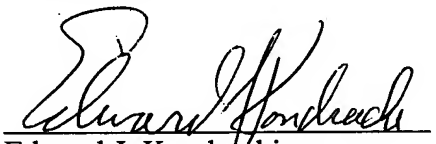
REMARKS

Claims 1-12 are pending. These claims have been amended to place them in a form which better conforms with U.S. claim practice. The specification has also been amended to include section headers, and a new abstract has been provided.

It is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application, including extension of time fees, to Deposit Account No. 50-1165 (Attorney Docket No. T2147-907715) and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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Marked-Up Version of the Amended Claims

1. (Amended) A coherence [Coherence] controller [(64) adapted for being] connected to at least one multiprocessor within a local module, said multiprocessor including a local main memory and a plurality of processors [(40, 40')] each equipped with a cache memory [(42, 42') and with at least one local main memory (44) in order to define a local module (50) of basic multiprocessors (60)], said coherence controller [(64) including] comprising:

a cache filter directory [(84) comprising] including a first filter directory [SF designed to guarantee] for guaranteeing coherence between the local main memory [(44)] and the cache [memories (42, 42')] memory in each of the processors of the local module[, characterized in that it also includes];

a complementary filter directory for tracking locations of lines or blocks of the local main memory copied from the local module into at least one external module and for guaranteeing coherence between the local main memory and the cache in each of the processors of the local module and said at least one external module; and an external port [(99) adapted for being] connected to said at least one external [multiprocessor] module [(51, 52, 53) identical to or compatible with said local module (50), the cache filter directory [(84) including].

[a complementary filter directory ED for keeping track of the coordinates, particularly the addresses, of the lines or blocks of the local main memory (44) copied from the local module (50) into an external module (51, 52, 53) and guaranteeing coherence between the local main memory (44) and the cache memories (42, 42') of the local module (50) and the external modules (51, 52, 53).]

2. (Amended) A coherence [Coherence] controller [(64)] according to claim 1, [characterized in that it also includes] wherein the cache filter directory includes:

an "n"-bit presence vector [(86),] where [N] n is [the] a number of [basic] multiprocessors in [a] the local module,

an ["N-1"] "n-1"-bit extension [(88)] of the presence vector, where [N] n-1 is [the] a total number of external modules [(51, 52, 53)] connected to the external port [(99)], and

an Exclusive status bit [(87)].

3. (Amended) A coherence [Coherence] controller [(64)] according to claim 2, [characterized in that] wherein the external port [(99)] is connected directly or indirectly to [the] said at least one external module [modules (51, 52, 53)] via an external two-point link [(55)].

4. (Amended) A coherence [Coherence] controller [(64)] according to claim 2, [characterized in that it includes] further comprising:

"n" control units [PU (80-83) of local ports (90-93)] connected to the n [basic] multiprocessors [(60-63) of] in the local module [(50)],

a control unit XPU [(89) of] connected to the external port [(99)], and

a common control unit [ILU of] containing the cache filter directory [directories SF/ED (84)].

5. (Amended) A coherence [Coherence] controller [(64)] according to claim 4, [characterized in that] wherein the control unit XPU [(89) of the external port] and the

"n" control units [PU (80-83) of the local ports] are compatible with one another and use at least substantially similar[, largely common] protocols.

6. (Amended) A multiprocessor [Multiprocessor] module [(50), characterized in that it includes a plurality of multiprocessors (60-63) equipped with at least one cache memory (42, 42') and at least one main memory (44) and] connected to a coherence controller [(64) according to any of claims 1 through 5] as recited in claim 1.

7. (Amended) A multiprocessor [Multiprocessor] system with a multimodule architecture, [characterized in that it includes] comprising:

at least two multiprocessor modules [(50-53) according to] as recited in claim 6, connected to one another directly or indirectly through [the] external ports [(99)] of [the] coherence controllers [(64)] located within said at least two multiprocessor modules.

8. (Amended) A multiprocessor [Multiprocessor] system according to claim 7, [characterized in that] wherein said external ports [(99)] are connected to one another through a switching device or router [(54)].

9. (Amended) A multiprocessor [Multiprocessor] system according to claim 8, [characterized in that] wherein the switching device or router [(54)] includes [means for managing and/or filtering] a unit which manages and/or filters [the] data and/or requests in transit between said at least two multiprocessor modules.

10. (Amended) A large-scale [Large-scale] symmetric multiprocessor server with a multimodule architecture [characterized in that it comprises], comprising:

["N"] a plurality of multiprocessor modules [(50-53) that are identical or compatible with one another, each module comprising], at least a first of said multiprocessor modules including:

a plurality of ["n" basic] multiprocessors [(60-63)] each equipped with at least one cache memory [(42)] and at least one local main memory [(44)], and [connected to]

a local coherence controller (64) connected to said multiprocessors and including a local cache filter directory [SF designed to guarantee] for guaranteeing local coherence between the local main memory and the cache memories [of] in each of said multiprocessors [the module, hereinafter called the local module, each], said local coherence controller [(64) being] connected [by an external two-point link (55), possibly via a switching device or router (54),] to at least a second one of said multiprocessor modules [module (51, 52, 53) outside said local module],

wherein the coherence controller [(64) including] further includes:

a complementary cache filter directory [ED for keeping track of the coordinates, particularly the addresses, of the] for tracking a location of memory lines or blocks copied from [the local] said first multiprocessor module to the second one of said multiprocessor modules [an external module] and for guaranteeing coherence between the local main memory [(44)] and the cache memories [(42, 42')] in each of the multiprocessors in [of the local] said first module [(50)] and [the external modules (51, 52, 53)] the second one of said multiprocessor modules.

11. (Amended) A multiprocessor [Multiprocessor] server with a multimodule architecture according to claim 10, [characterized in that each] wherein the coherence controller [(64)] includes:

an "n"-bit presence vector [(86) designed to indicate] which indicates [the] presence or absence of a copy of a memory block or line in the cache memories of the [local basic] multiprocessors,

an ["N-1"] "n-1"-bit extension [(88)] of the presence vector [designed to indicate the] which indicates presence or absence of a copy of a memory block or line in [the] cache memories of [the] multiprocessors [of the external modules (51, 52, 53)] in the second one of said multiprocessor modules, and

an Exclusive status bit [(87)].

12. (Amended) A multiprocessor [Multiprocessor] server with a multimodule architecture according to claim 10, [characterized in that the] further comprising:

a switching device or router [(54)] which connects the first multiprocessor module with the second one of said multiprocessor modules, said switching device or router including [includes means for managing and/or filtering the] a unit which manages and/or filters data and/or requests in transit between the first multiprocessor module and the second one of said multiprocessor modules.